



SSC8025GN2

P-Channel Enhancement Mode MOSFET

➤ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$	I_D
-20V	$\pm 12V$	27m Ω @-4V5	-7A
		44m Ω @-2V5	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

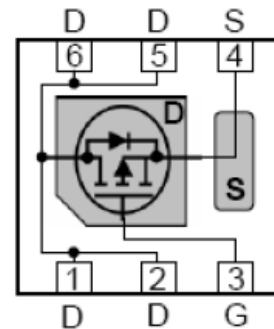
➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

➤ Ordering Information

Device	Package	Shipping
SSC8025GN2	DFN2020-6L	3000/Reel

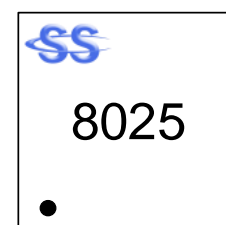
➤ Pin Configuration



DFN2020-6L (Top View)



Bottom View



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^d	$T_C=25^{\circ}\text{C}$	-7
		$T_C=100^{\circ}\text{C}$	-3.9
I_{DM}	Pulsed Drain Current ^b	-27	A
P_D	Power Dissipation ^c	$T_C=25^{\circ}\text{C}$	2.12
		$T_C=100^{\circ}\text{C}$	0.85
T_J	Operation junction temperature	-55~150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55~150	

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	59	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(\text{MAX})}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- The maximum current rating is package limited.

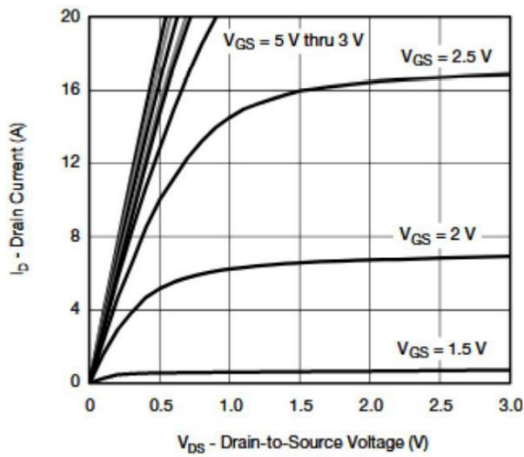


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

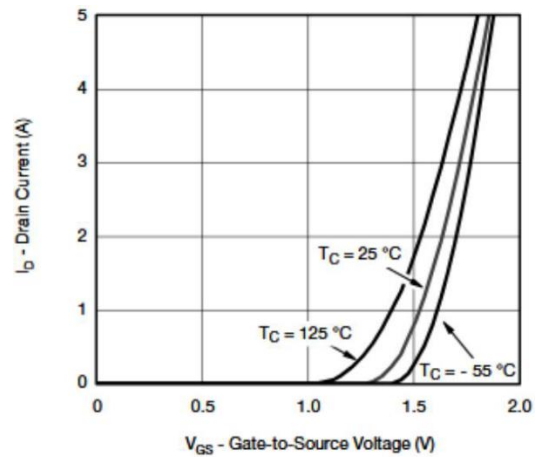
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.7	-1	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -4A		27	36	mΩ
		V _{GS} = -2.5V, I _D = -3A		44	60	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±12V, V _{DS} = 0V			±100	nA
Transconductance	G _{FS}	V _{DS} = -5V, I _D = -3.5A		9		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -1.6A		-0.75	-1.2	V
Input Capacitance	C _{ISS}	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		830		pF
Output Capacitance	C _{OSS}			190		
Reverse Transfer Capacitance	C _{RSS}			197		
Total Gate Charge	Q _G	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -4A		15		nC
Gate to Source Charge	Q _{GS}			2.3		
Gate to Drain Charge	Q _{GD}			2.2		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = -4.5V, V _{DS} = -10V, R _L = 4Ω, R _G = 1Ω I _D = -2.5A		10		ns
Rise Time	T _r			30		
Turn-off Delay Time	T _{D(OFF)}			20		
Fall Time	T _f			11		



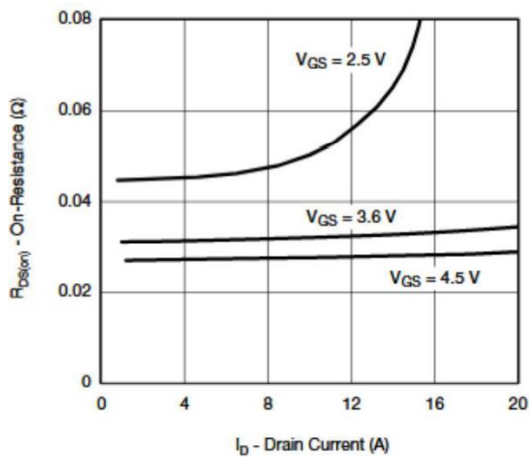
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



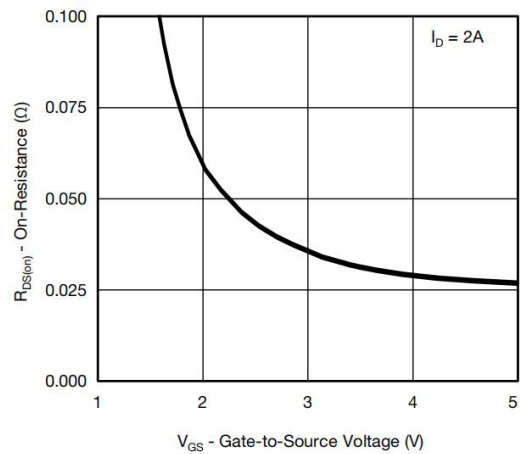
Output Characteristics



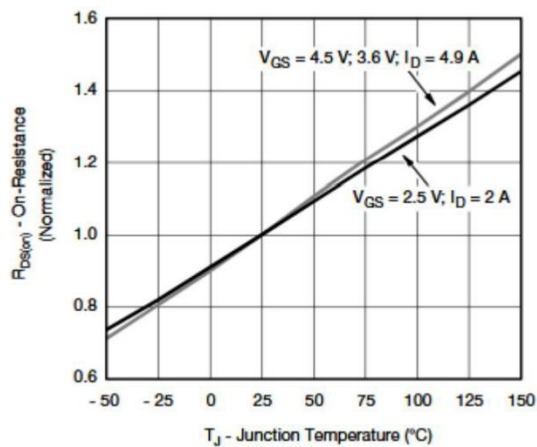
Transfer Characteristics



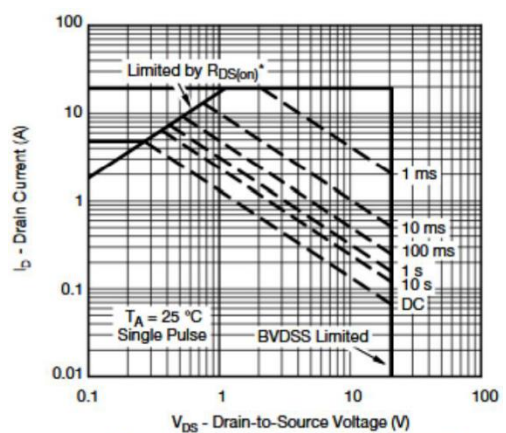
On Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

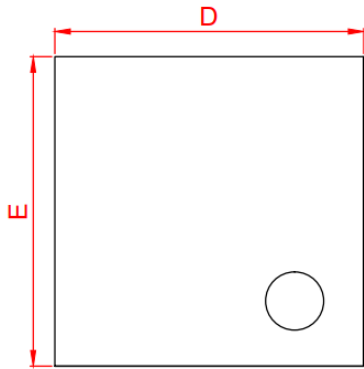


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

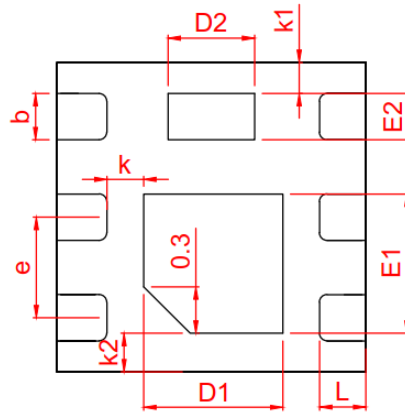
Safe Operating Area, Junction-to-Ambient



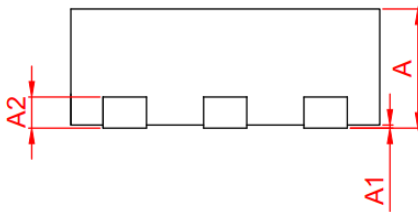
➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
* A1	0.00	0.02	0.05
* b	0.25	0.30	0.35
* A2	0.152 BSC		
* D	1.95	2.00	2.05
* E	1.95	2.00	2.05
* E1	0.80	0.90	1.00
* E2	0.25	0.30	0.35
* D1	0.80	0.90	1.00
* D2	0.46	0.56	0.66
* e	0.65 REF		
* L	0.25	0.30	0.35
* K	0.20	0.25	0.30
* K1	0.15	0.20	0.25
* K2	0.20	0.25	0.30

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